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vBNG dataplane in **P4**-programmable **FPGA**-based acceleration card

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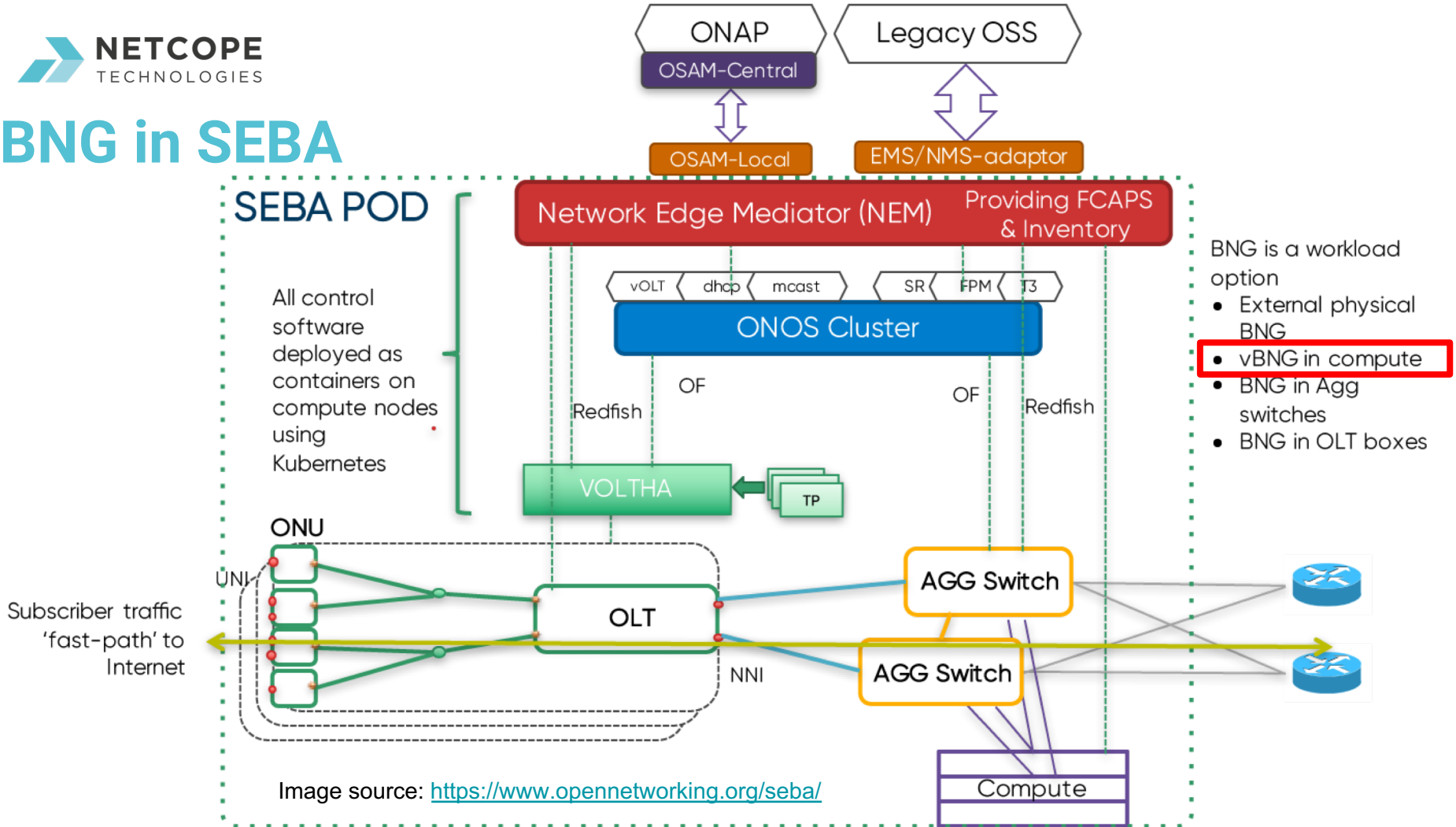
BNG in SEBA



BNG is a workload option

- External physical BNG
- vBNG in compute
- BNG in Agg switches
- BNG in OLT boxes

Image source: https://www.opennetworking.org/seba/

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vBNG in compute

- ✓ Software flexibility - upgrade, bugfix, customize
- ✓ Scales with the number of servers (assuming load balancing)
- ✓ Can be standalone

- CAPEX, OPEX per Gbps?

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Our plan

FPGA accelerators available as a config option when buying a server.

Use commodity servers with FPGA accelerator to run optimized vBNG.

Use P4 to implement the vBNG data plane in FPGA.

Use CPU cores to run vBNG control plane.

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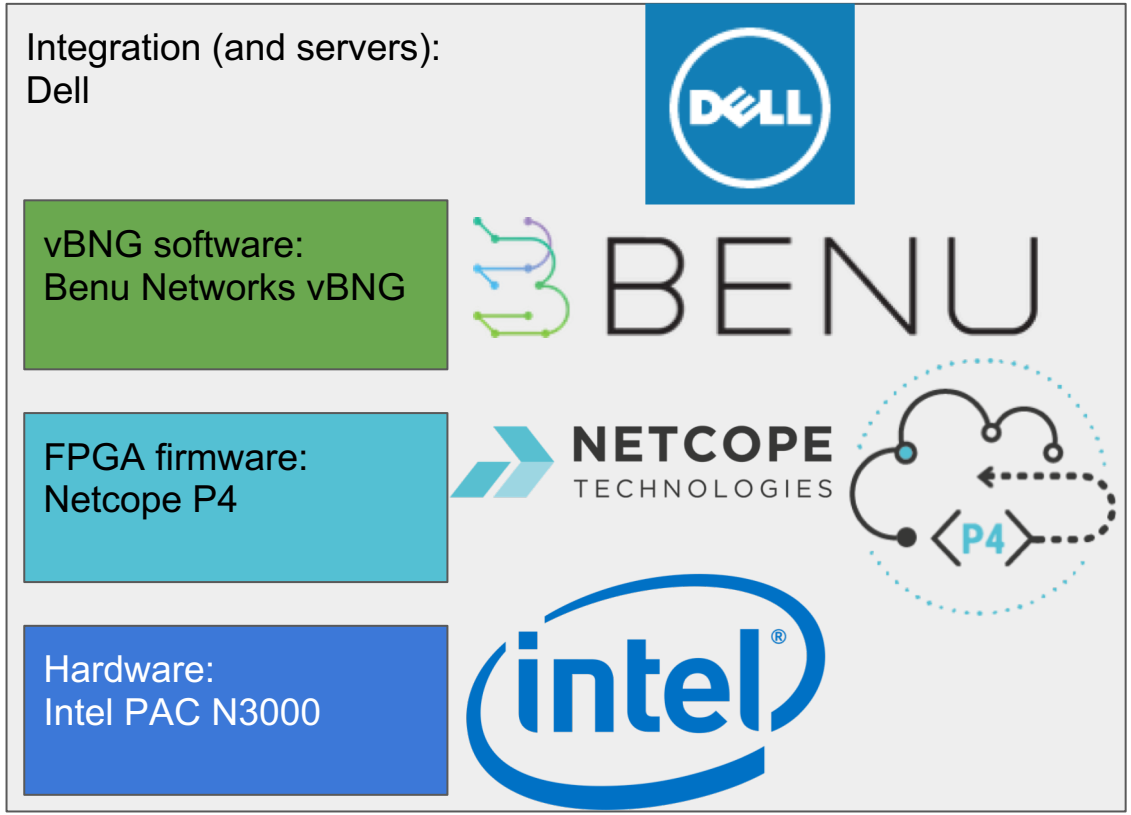
Ecosystem



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vBNG Architecture

Most traffic **processed only in FPGA** (**red**)

First packets and exception traffic (ex. DHCP) **forwarded locally** to control plane (**green**)

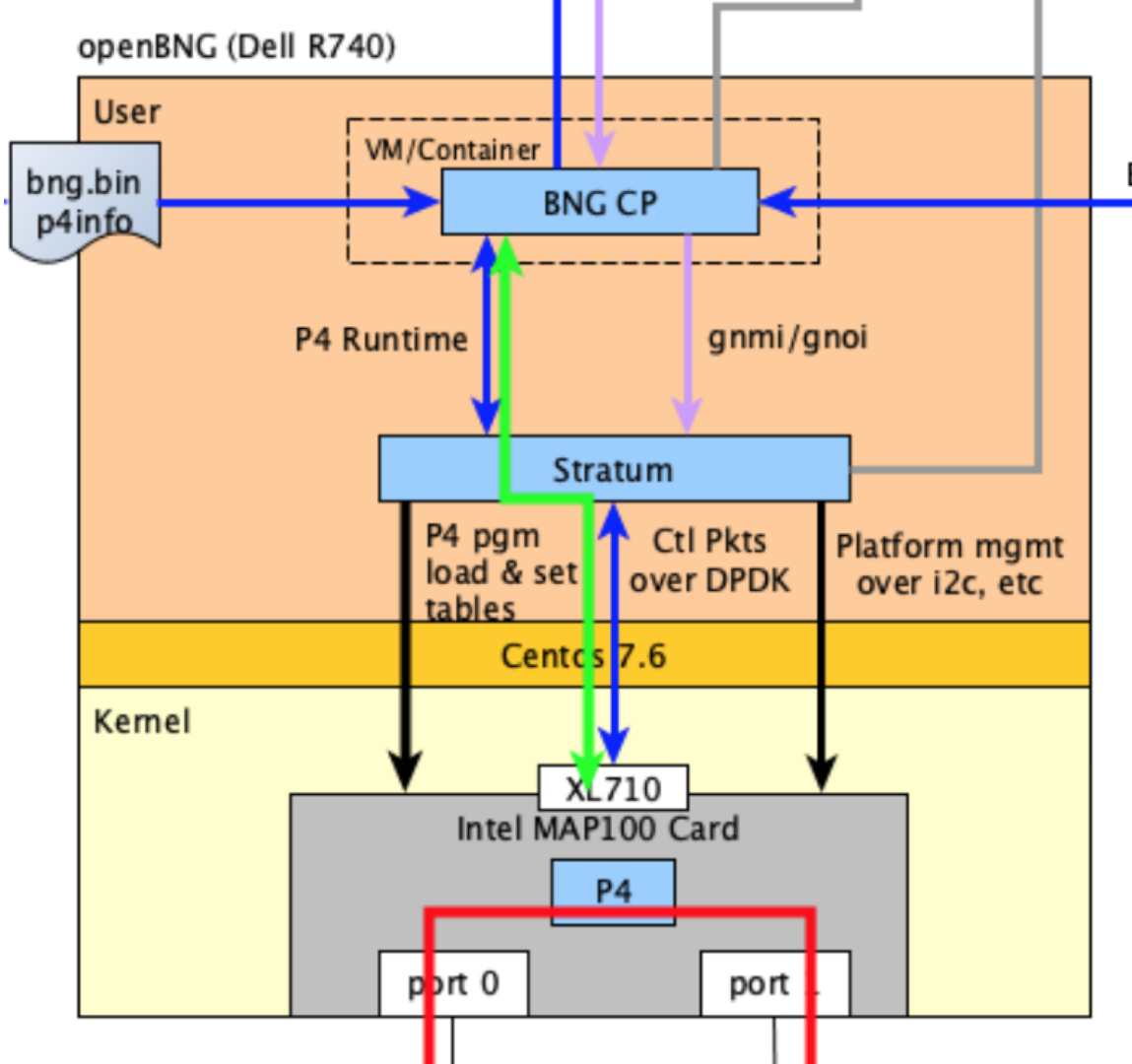

Image credit: Craig Stevens, Dell

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vBNG pipeline in FPGA

Using P4 code from https://github.com/opencord/p4se

- Complex
  - ~30 Match Action Tables
  - ~25 Counter arrays
  - Many `#ifdef`s (INT, IPv6, SPGW, VRF, …)
- Does not cover features outside P4 language spec (QoS)
  - Set as output metadata

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Results (focused at P4 on FPGA)

Features

Throughput

Subscribers

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Next Steps

Use on-board DRAM to implement

- Large-capacity tables
  - Millions of entries
  - => Support more subscribers
- HQoS
  - Separate FPGA module, controlled by P4 output metadata

Full integration

- Using open standards for extensibility (P4, P4Runtime, DPDK)

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Thank you for attention.

www.netcope.com

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