Towards Programmable Scheduling: PIFO Implementation on NetFPGA

S. Ibanez, A. Dalleggio, G. Brebner, and N. McKeown

April 20, 2018

1 Abstract

The packet processing capabilities of the P4 language are second to none. That being said, there has been very little discussion around ways to program the traffic management capabilities of network devices. Modern programmable switches offer a small menu of common scheduling algorithms, but provide no mechanism for allowing network operators to define their own algorithms. The PIFO (Push-In-First-Out) queue was recently proposed as a convenient abstraction that can be used to implement many different scheduling algorithms, and hence provides a mechanism to make packet scheduling programmable [1]. PIFOs differ from traditional scheduling mechanisms because they decide the packet's scheduling order at the time of enqueue rather than as the packet leaves the queue.

This demonstration will showcase the first practical PIFO design for an FPGA target. The design can be scaled to support various line rates and we will demonstrate how our PIFO can be used to implement various common scheduling algorithms at 10Gb/s using the NetFPGA SUME platform.

This work helps us to better understand the hardware requirements to support programmable scheduling and allows us to start considering how we might extend the P4 language to describe traffic management.

2 Presenters

Stephen Ibanez (Stanford), Anthony Dalleggio (NYU), Gordon Brebner (Xilinx Labs), and Nick McKeown (Stanford).

References

[1] Anirudh Sivaraman, Suvinay Subramanian, Mohammad Alizadeh, Sharad Chole, Shang-Tse Chuang, Anurag Agrawal, Hari Balakrishnan, Tom Edsall, Sachin Katti, and Nick McKeown. Programmable packet scheduling at line rate. In *Proceedings of the 2016 ACM SIGCOMM Conference*, pages 44–57. ACM, 2016.