Using P4 for converged and programmable XHaul in mobile RAN

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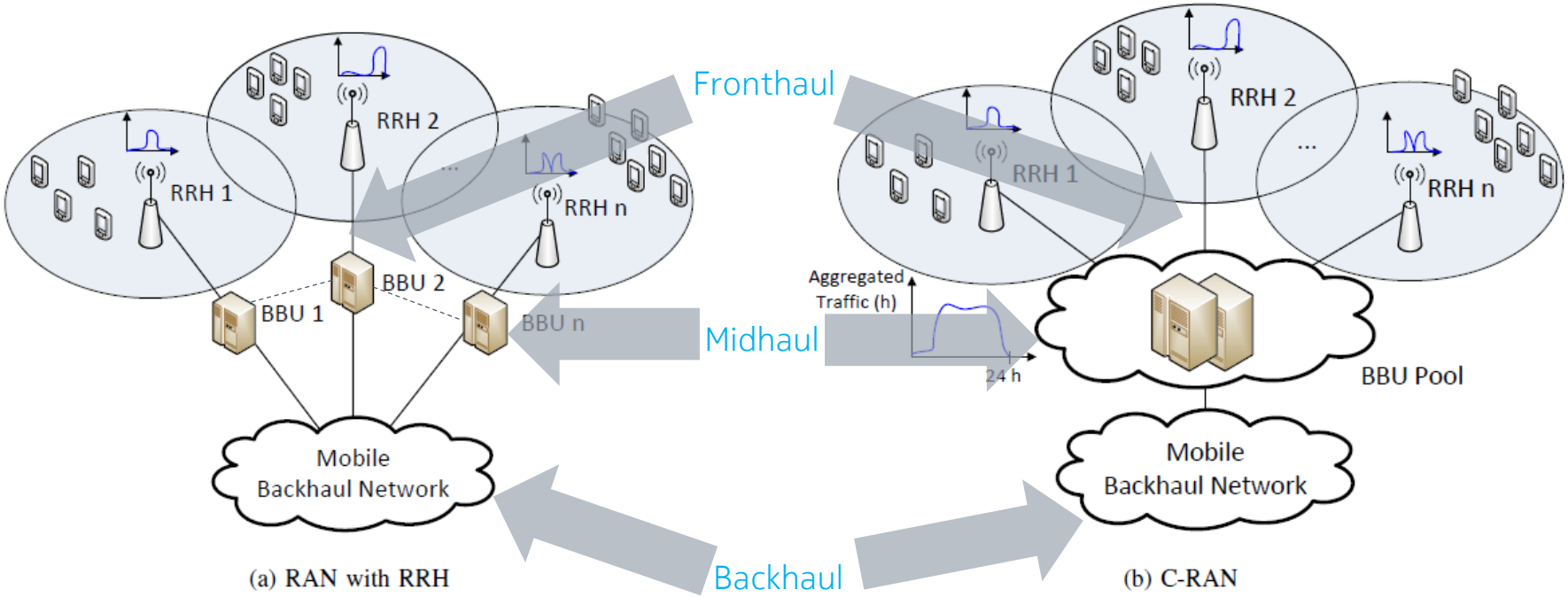
XHaul Overview



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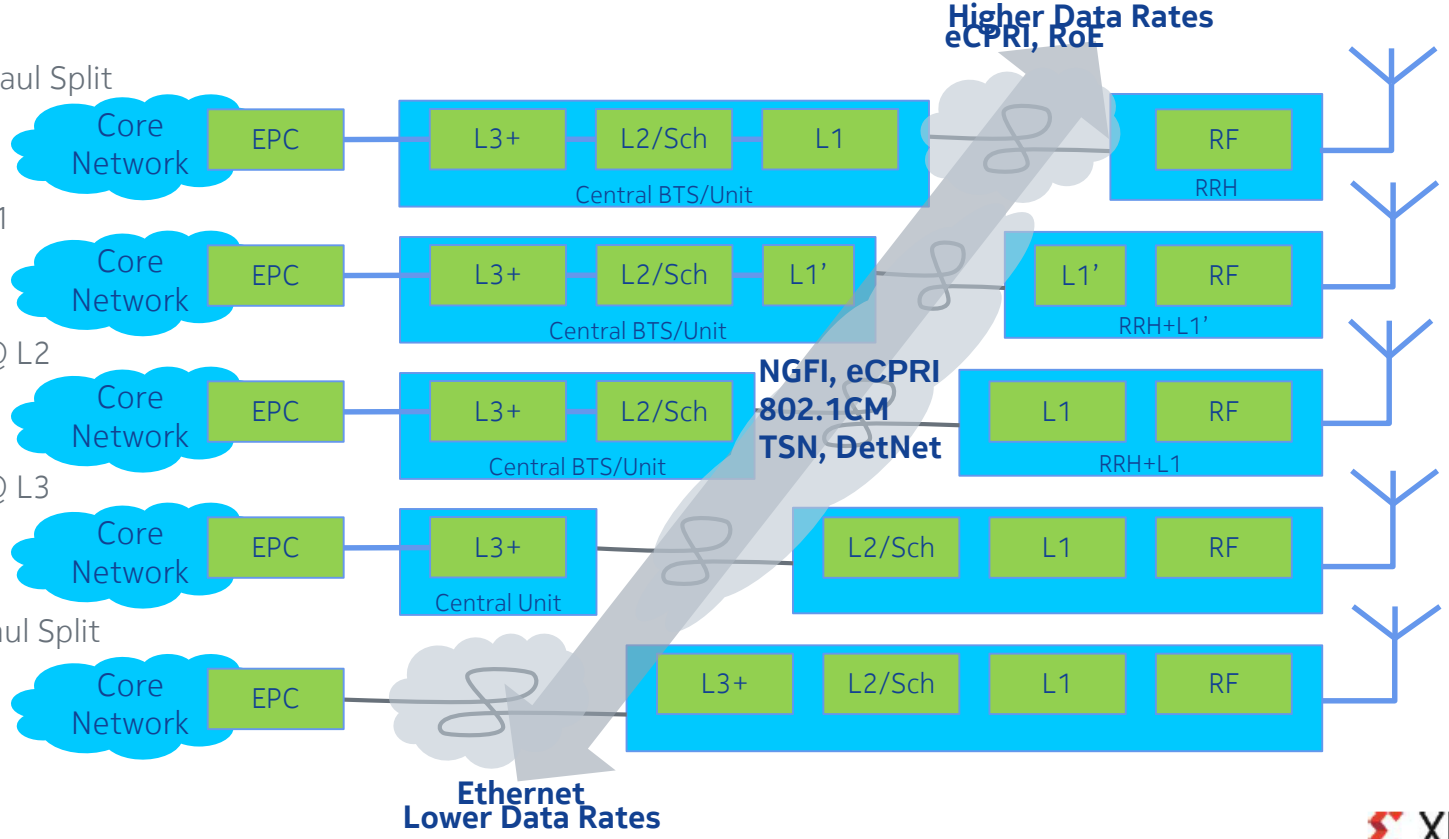
Converged XHaul Challenges

1. Fronthaul Split
2. Split L1
3. Split @ L2
4. Split @ L3
5. Backhaul Split



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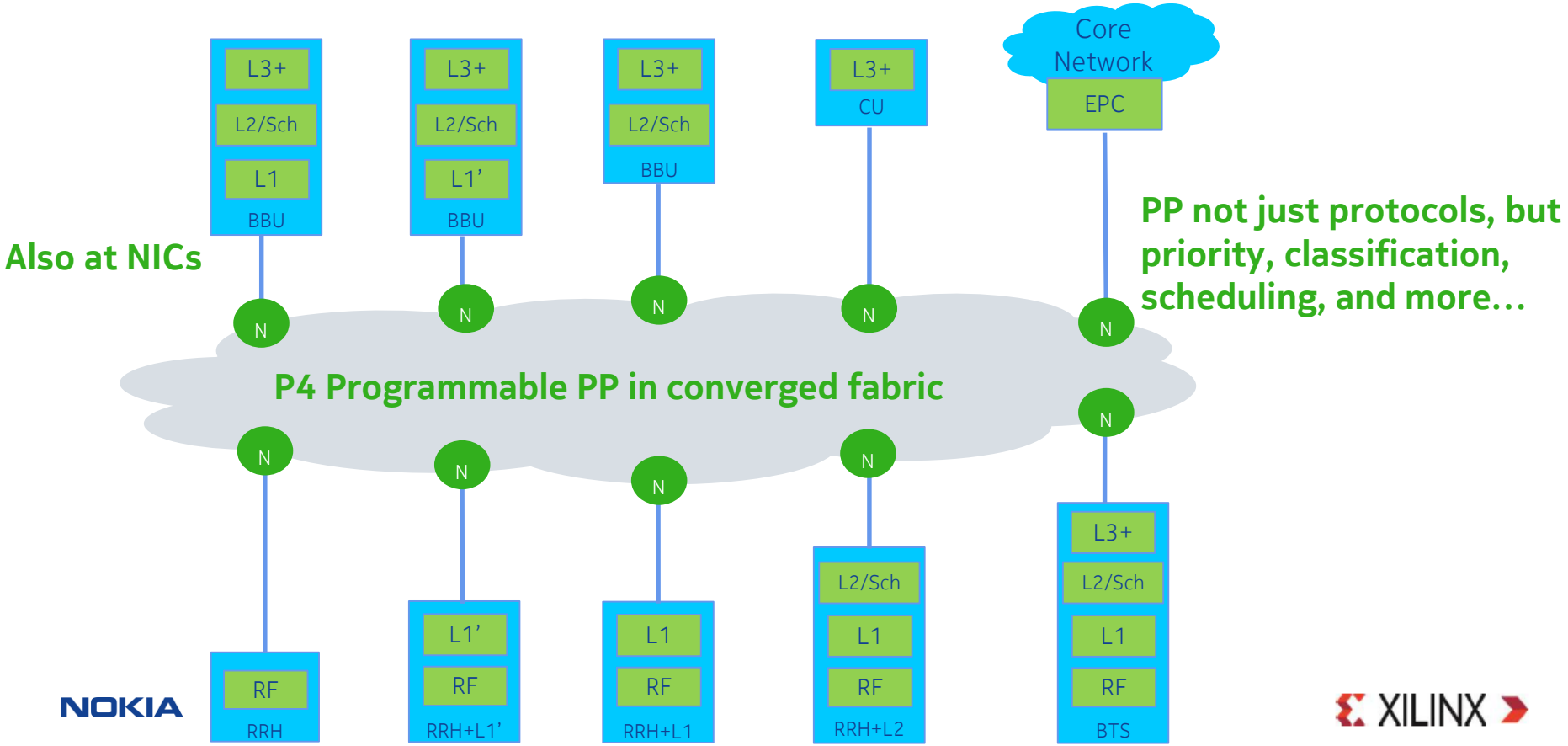
P4 Converged Solution



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What Does P4 Solve for X-Haul?

Issues	Resolution Using P4
No single right solution. Multiple options with diverse requirements.	Single converged HW but customizable solutions using programmable P4 SW
How to inter-operate and upgrade?	Enhance NIC + fabric to inter-operate with SW upgrade.
Silicon follows standardization, which is far away	No need to wait. Evolve with standards and new protocols as they emerge.

Churns  Good for using P4

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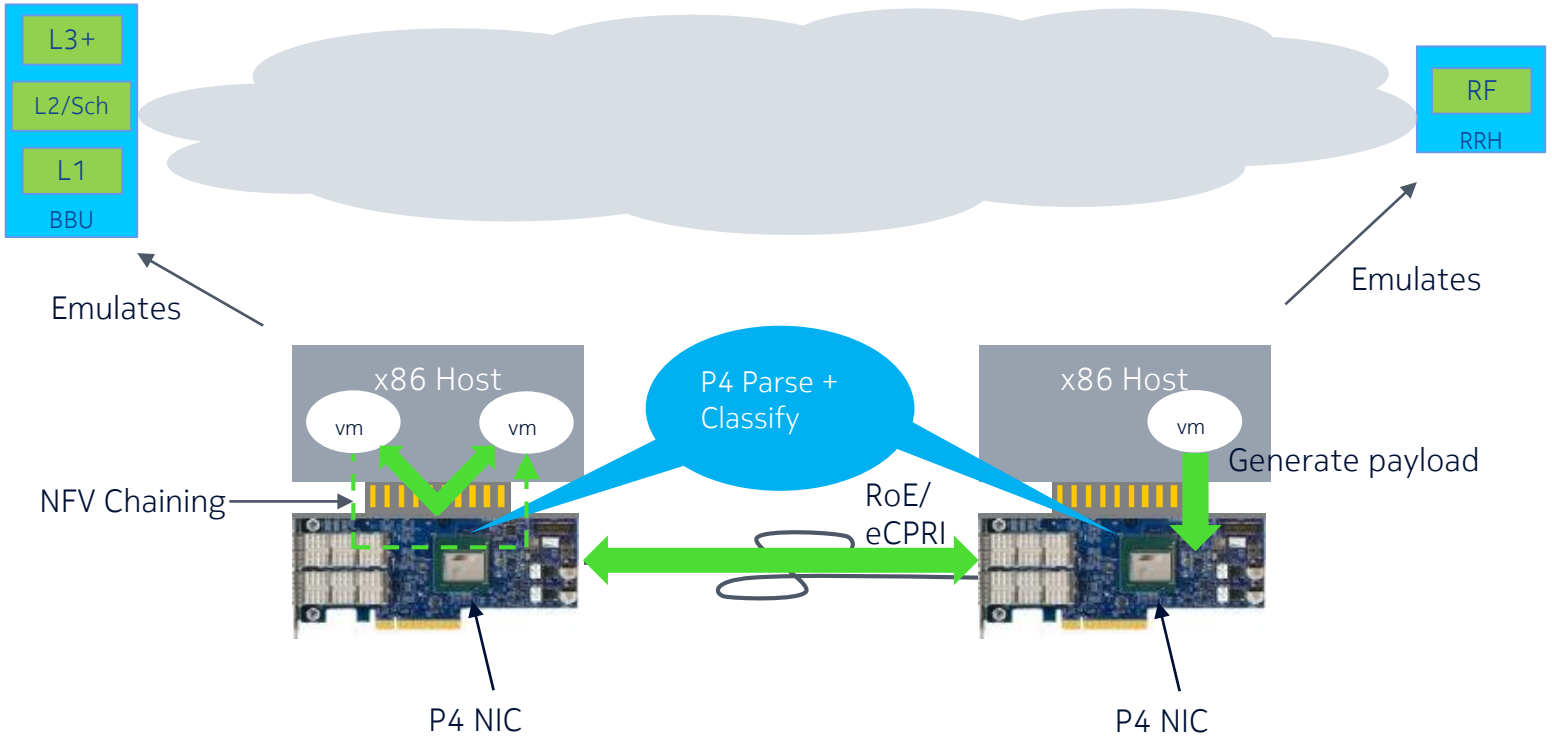
P4 XHaul PoC (RRH to BBU)



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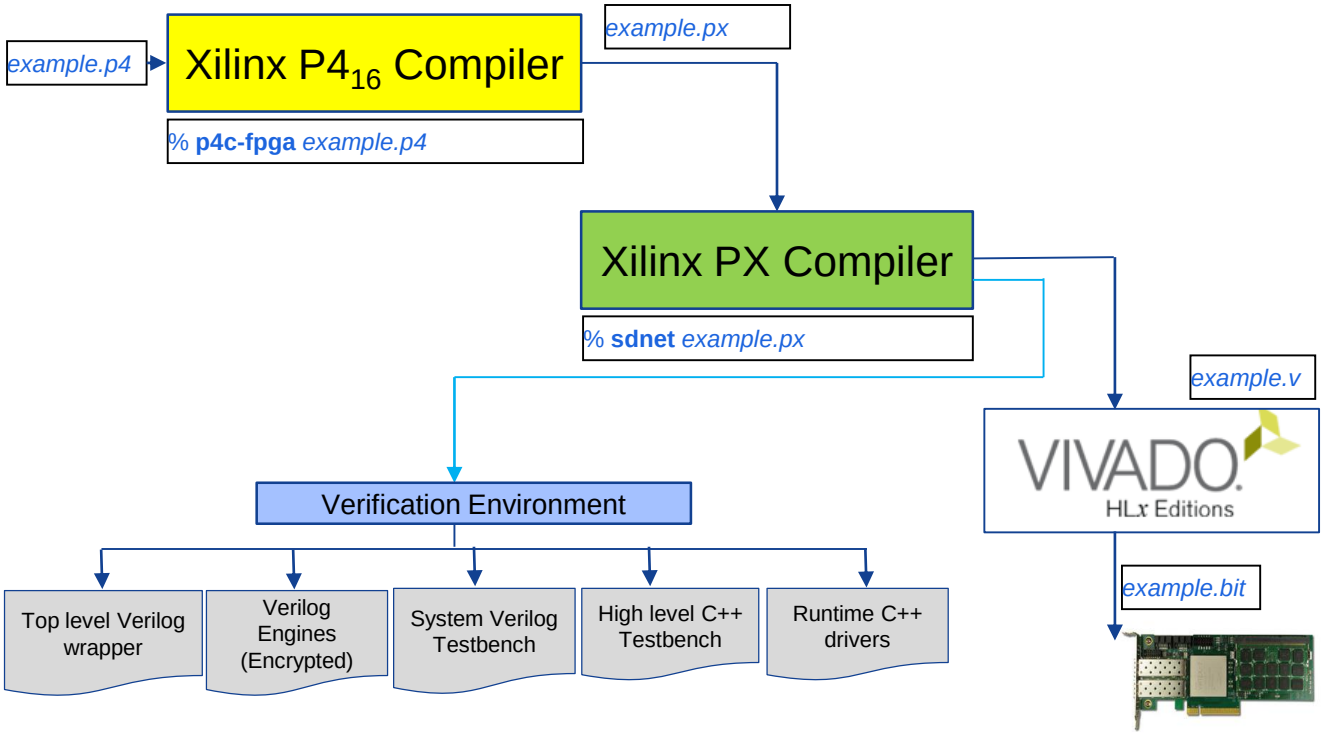
Current Xilinx P4 compilation (www.xilinx.com/sdnet)



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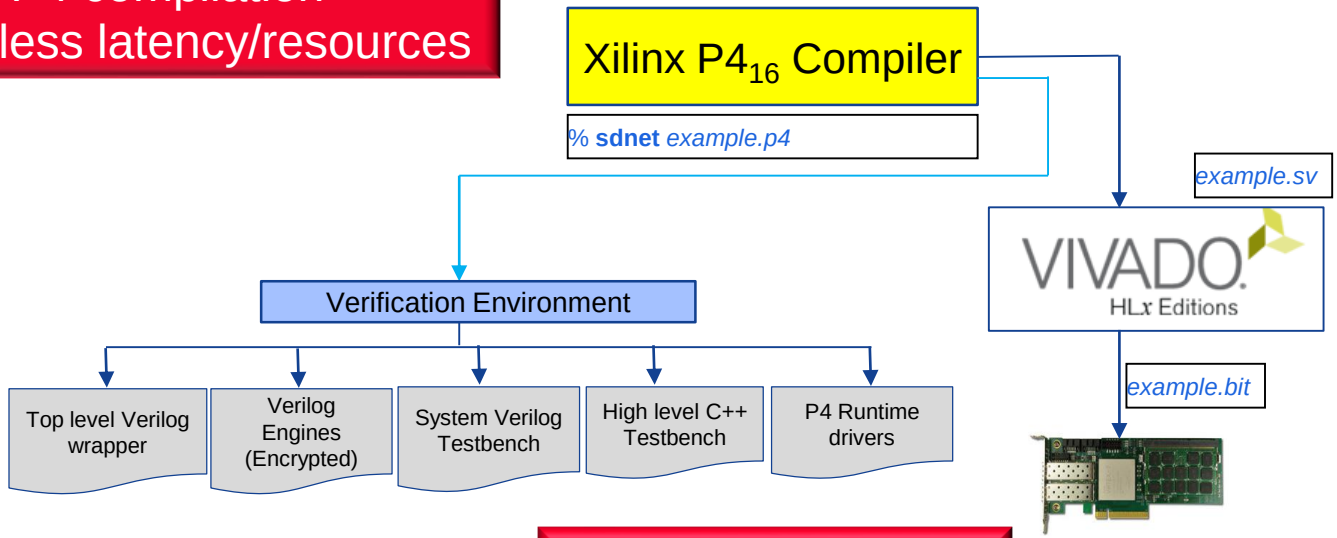
Next-generation Xilinx P4-SDNet compilation

Prototyped now, scheduled for release in November 2018

Optimization of data path:
Native P4 compilation
>50% less latency/resources



Open standard API:
P4 Runtime

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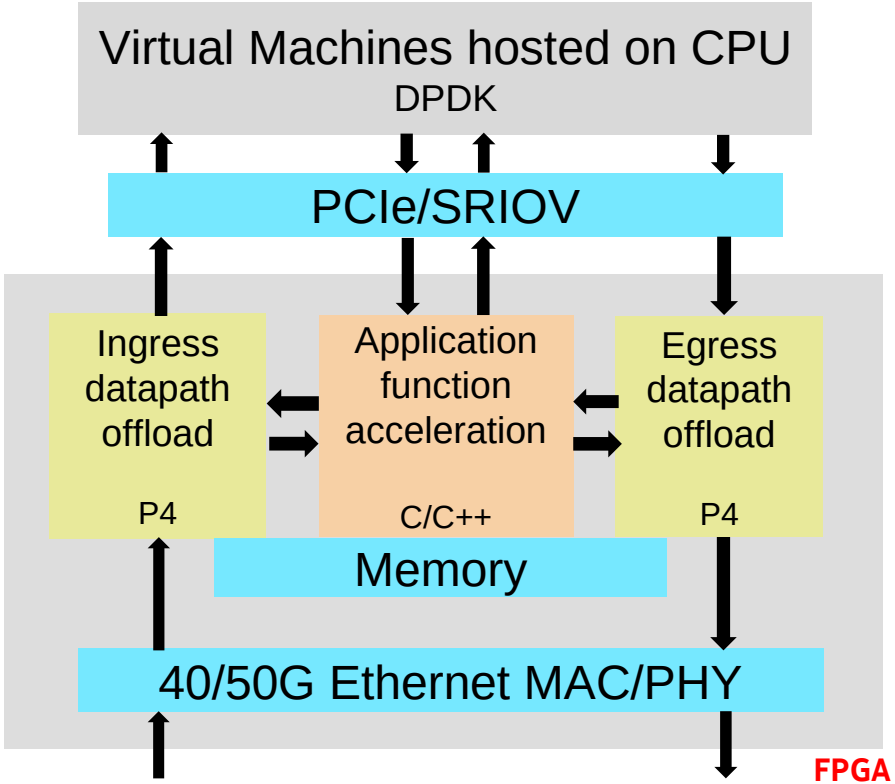
Xilinx Labs “Type 1, 2 and 3 NIC” prototype



	Description	Example features
Type 1	Basic Connectivity NIC	• Basic offloads (CHKS, LSO, RSS) • Single Root I/O Virtualization • Tunnel offloads (VXLAN, GRE)
Type 2	SmartNIC for Network Acceleration	• Encryption/Decryption (IPSec) • Virtual Switch offload (OVS) • Programmable tunnel types
Type 3	SmartNIC for Network + Compute Acceleration	• Inline Machine Learning • Inline Transcoding for Video • Database Analytics

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Summary and Suggestions

- P4 for RAN XHaul a good fit because of churns:
  - Multiple options, requirements and standardization work
  - Need HW before standardization
  - Convergence for economy of scale and operational efficiency

- Working PoC between RRH and BBU with Xilinx P4-programmed SmartNIC

- Suggestions for P4 community:
  - Support PP capability needs identified in emerging TSN and other work
  - NICs just as important as switches, so P4 NIC model as a future architecture?

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