A Heterogeneous Data Plane for Flexible P4 Processing

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- Main Ideas
  - Extend the processing limitation of a single target.
  - Combine multiple targets into a logical P4 pipeline.
  - Leverages a compiler that splits a P4 program along the different targets, based on their characteristics.
- Proof of Concept
  - Heterogeneous data plane comprising an ASIC and an FPGA.
  - The FPGA extends the memory limitation of the ASIC
  - The FPGA implements an ASIC unsupported P4 construct.