



NETRONOME

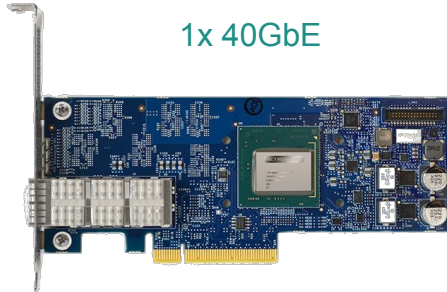
Mapping P4 to SmartNICs

Edwin Peer - 16 May 2017

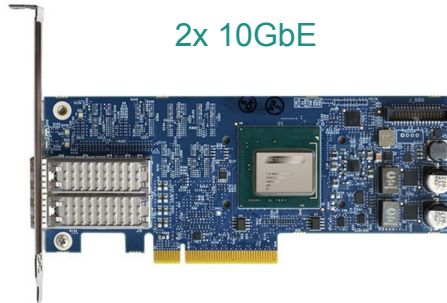
- ▶ SmartNIC Hardware
- ▶ Silicon Architecture
- ▶ Programming Model
- ▶ Mapping P4
- ▶ Results & Experience
- ▶ Further Reading / Q&A

- Optimized for standard server based cloud data centers
- Low profile half length PCIe form factor, power < 25W
- Based on Netronome's Network Flow Processor 4xxx silicon (72 cores x 8 threads each)
- 2GB DRAM for lookup tables / state tables (millions of entries)

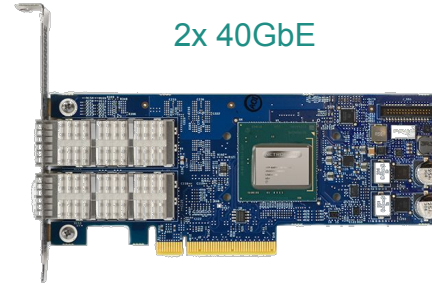
1x 40GbE



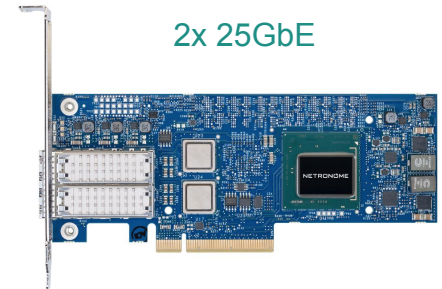
2x 10GbE



2x 40GbE

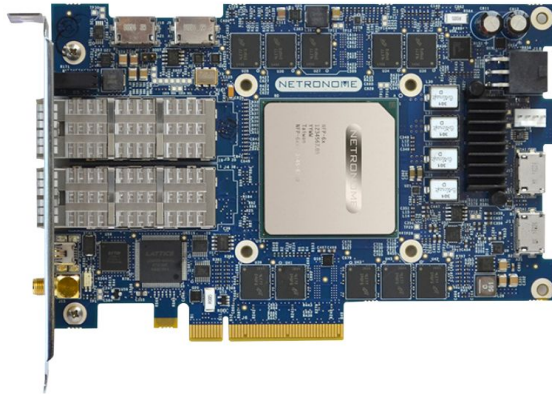


2x 25GbE

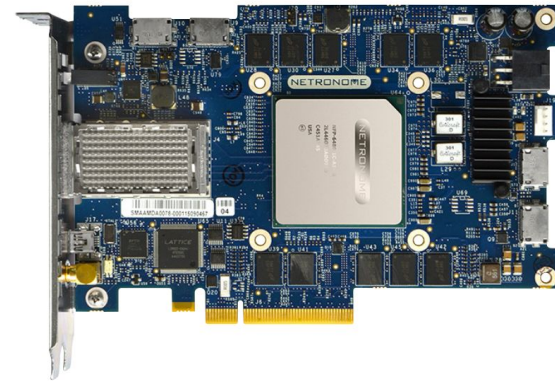


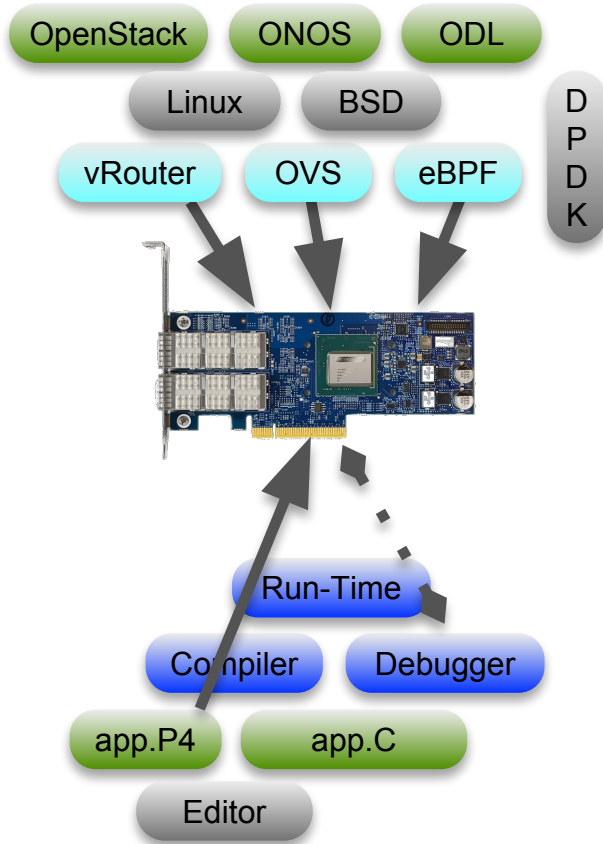
- Optimized for higher throughput requirements - middlebox, gateway, appliance, service node...
- Full height half length PCIe form factor
- Based on Netronome's Network Flow Processor 6xxx silicon (120 cores x 8 threads)
- Memory: 8GB of DDR3 DRAM @ 1866Mhz w/ECC
- Dual PCIe Gen3x8

2x40GbE (QSFP)

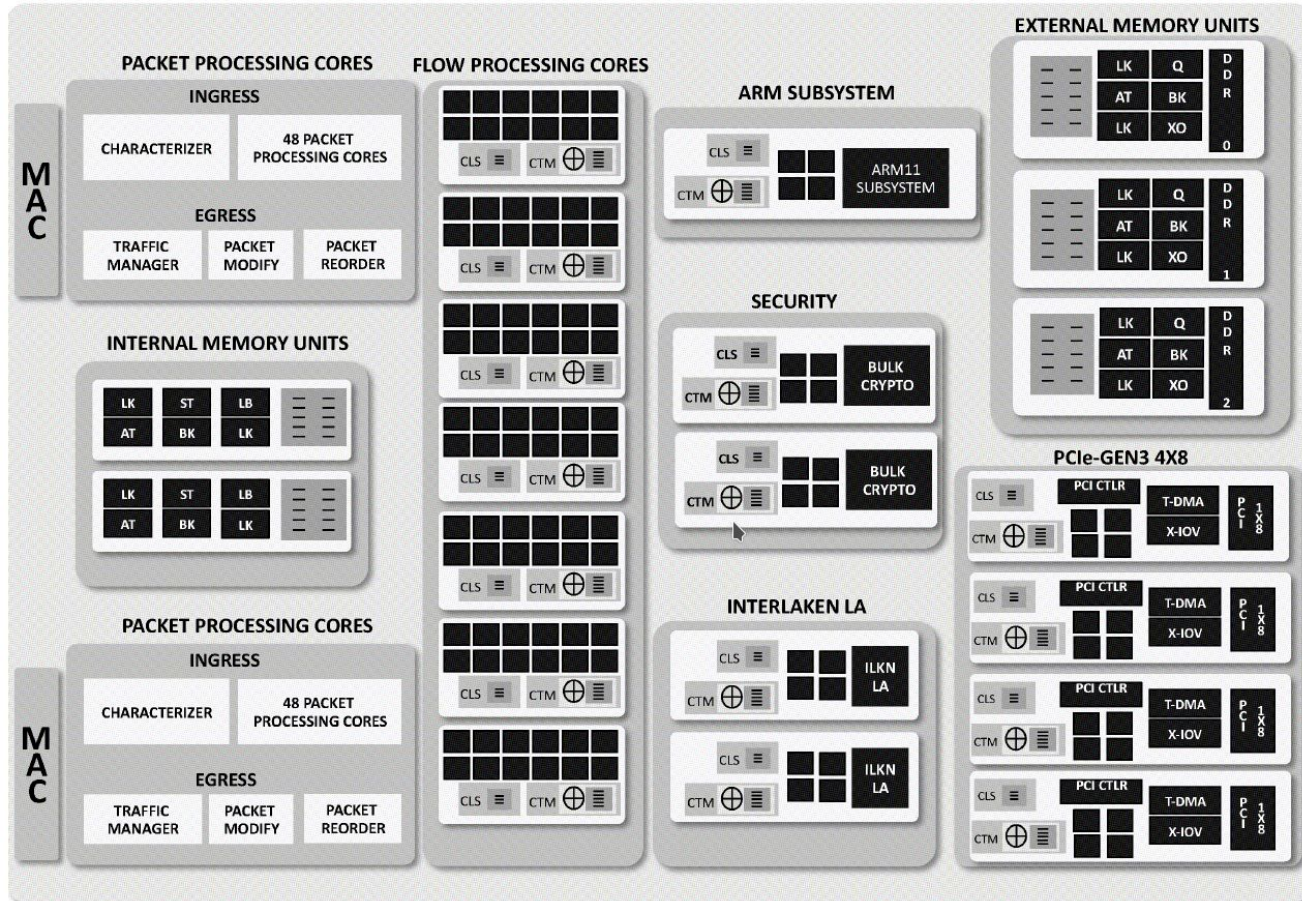


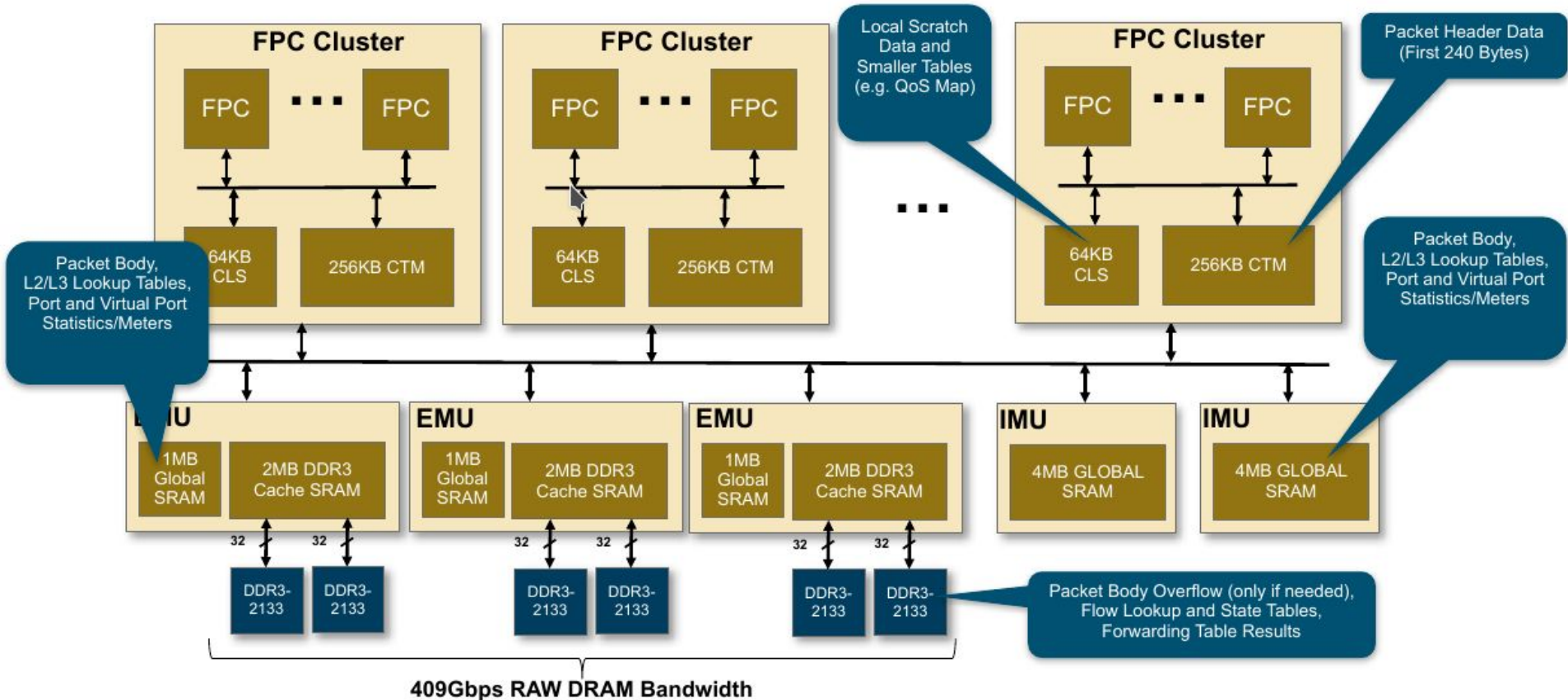
1x100GbE (CXP)





- Transparent acceleration of OVS / Contrail / eBPF
- SmartNIC with dynamic firmware
- Custom datapath in P4 and/or C





Network Flow Processor 4xxx / 6xxx

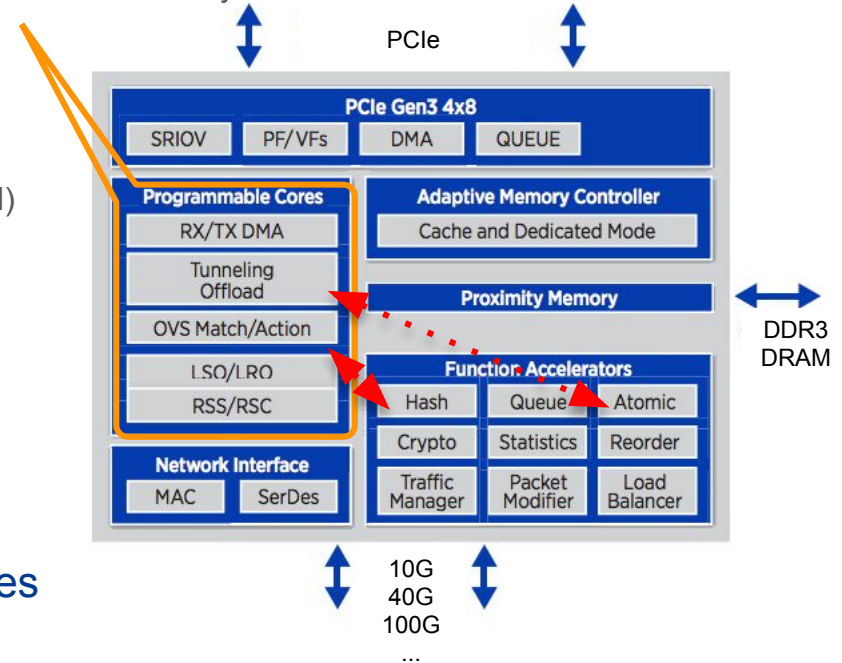
- ▶ Highly parallel multithreaded architecture (8 threads / core) for high throughput
- ▶ Purpose built Microengines / Flow Processing Cores (72 / 120) maximize flexibility
- ▶ H/W accelerators further maximize efficiency (throughput/watt)

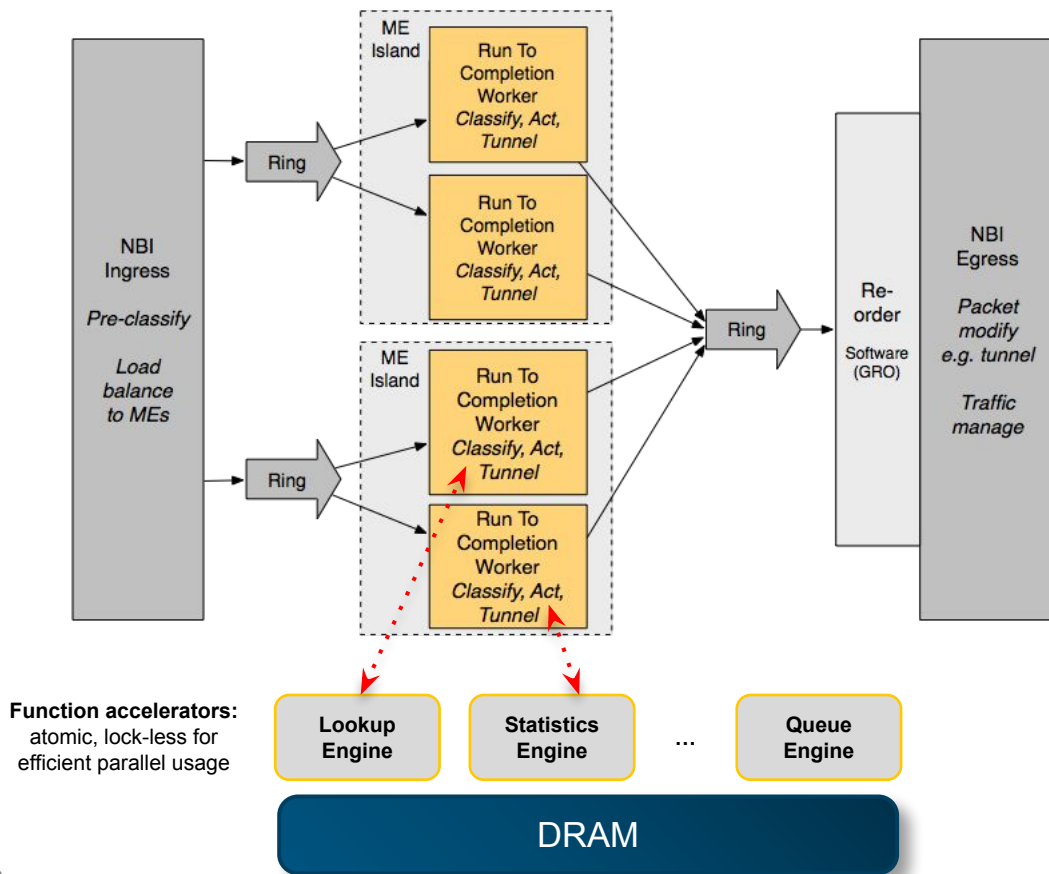
Fully software defined feature set - examples:

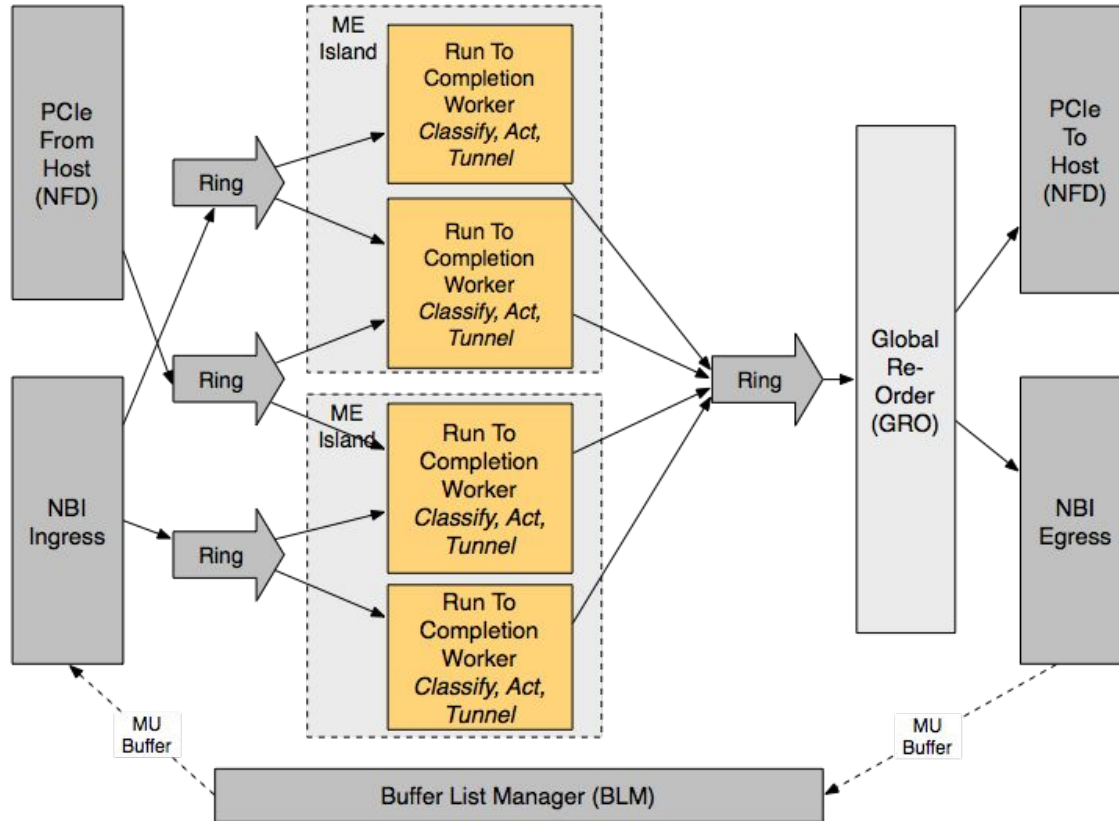
- ▶ Flexible tunneling support (e.g. VXLAN, GRE, VLAN, MPLS, NSH)
- ▶ Flexible Match/Action processing - many packet fields / protocols
- ▶ Highly scalable and fine grained security policies
- ▶ Network and PCIe SR-IOV / VirtIO RX/TX with stateless offloads
- ▶ Packet generation / reception with advanced statistics e.g. jitter
- ▶ Traffic directing (tapping / mirroring / steering / load balancing)

External DRAM accommodates millions of flows / rules

Convenient programmability using P4 and/or C

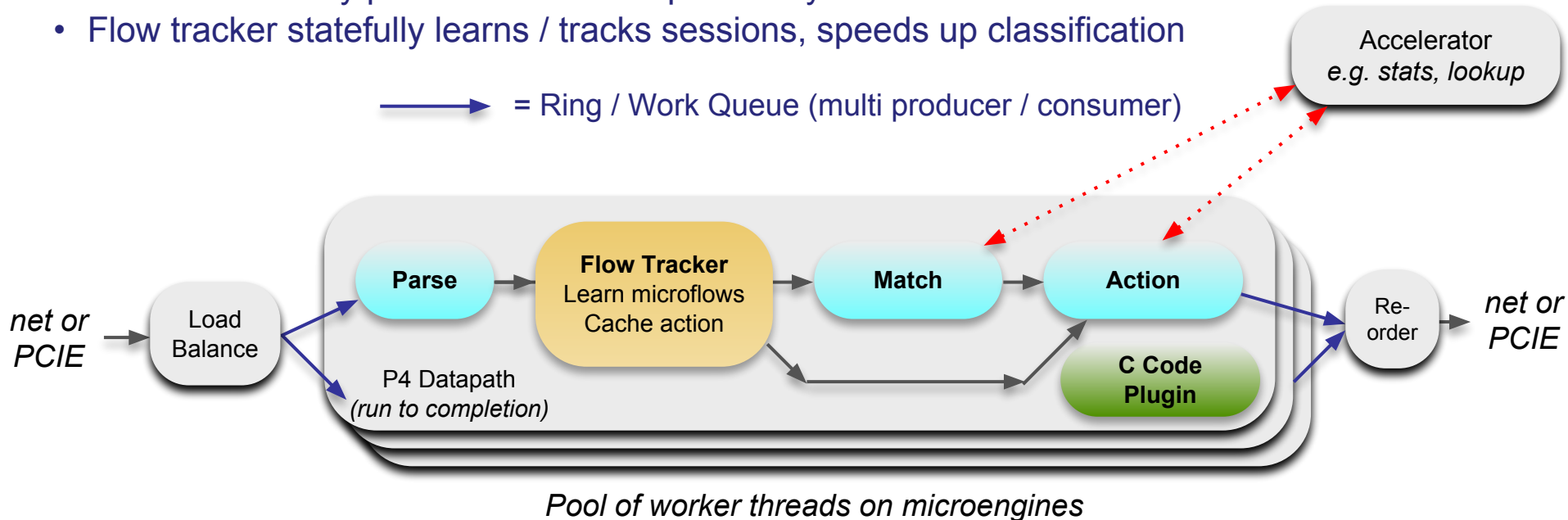


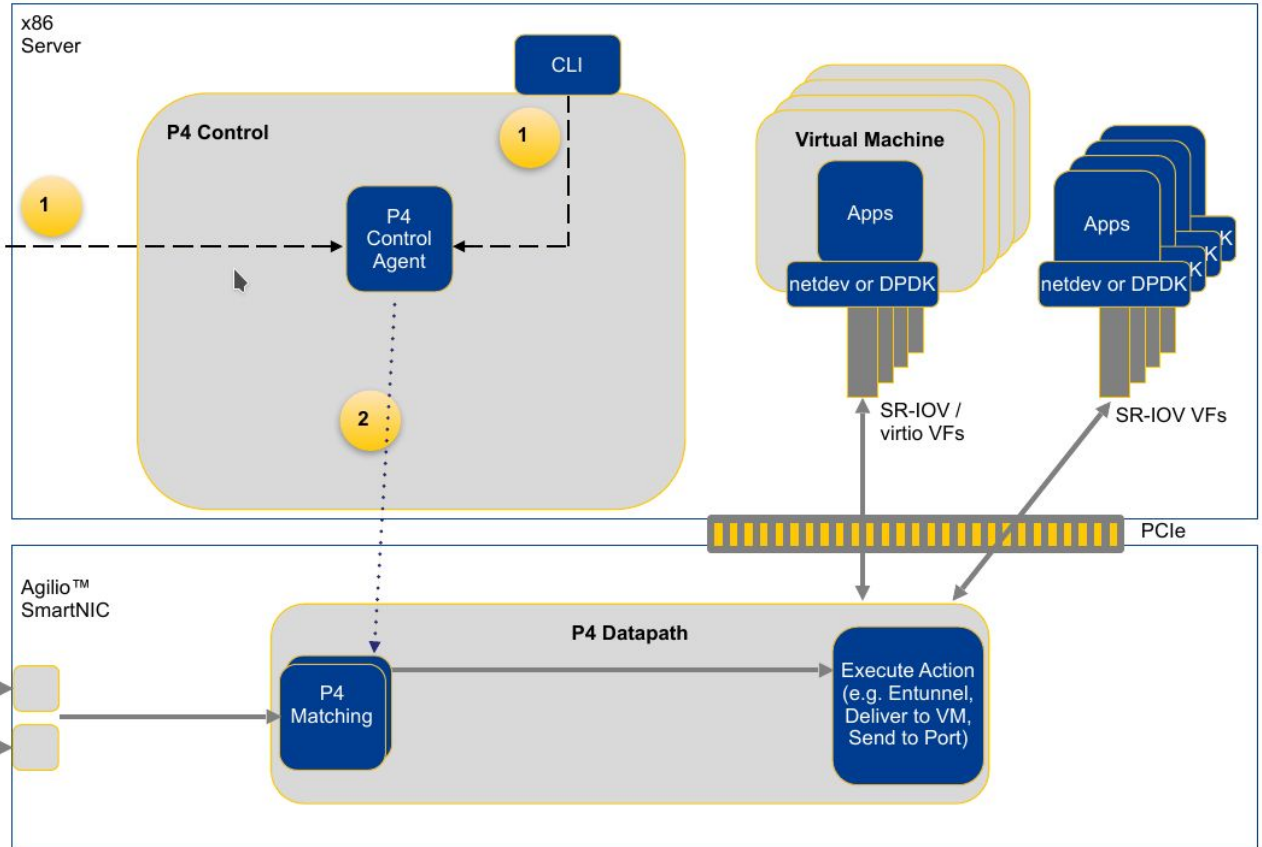




- Load balancer distributes each packet to next available thread for optimum throughput
- Hardware assisted reordering ensures packet order is maintained
- Matching performed using various algorithms, e.g. DRAM-backed “algorithmic TCAM”
- Actions efficiently performed in on-chip memory
- Flow tracker statefully learns / tracks sessions, speeds up classification

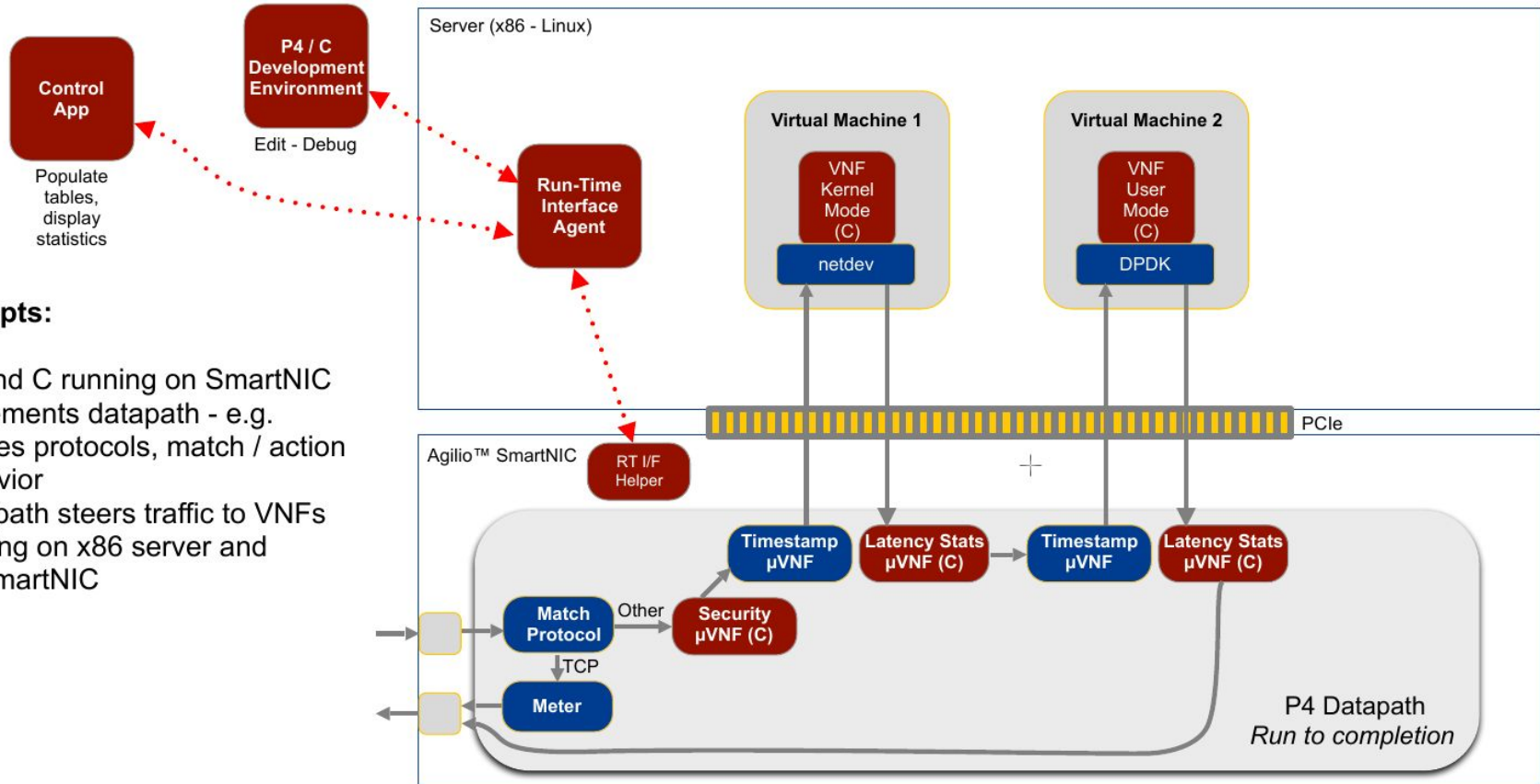
→ = Ring / Work Queue (multi producer / consumer)





Best of all worlds

- Performance of SR-IOV
- Flexibility of virtio (VM migration)
- Performance and CPU core saving of switching on SmartNIC



Concepts:

- P4 and C running on SmartNIC implements datapath - e.g. defines protocols, match / action behavior
- Datapath steers traffic to VNFs running on x86 server and on SmartNIC

P4 Debugging

C Programming

Graphical DP View

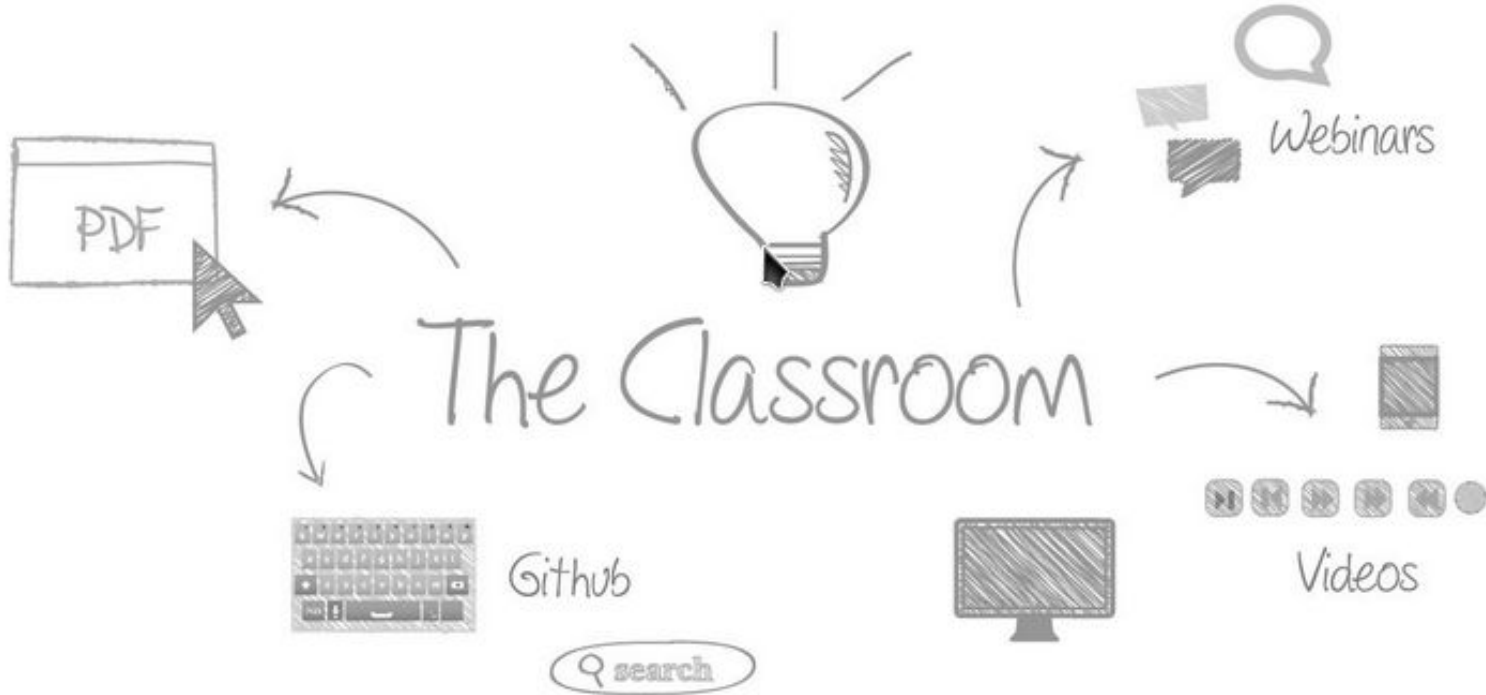
P4 Programming

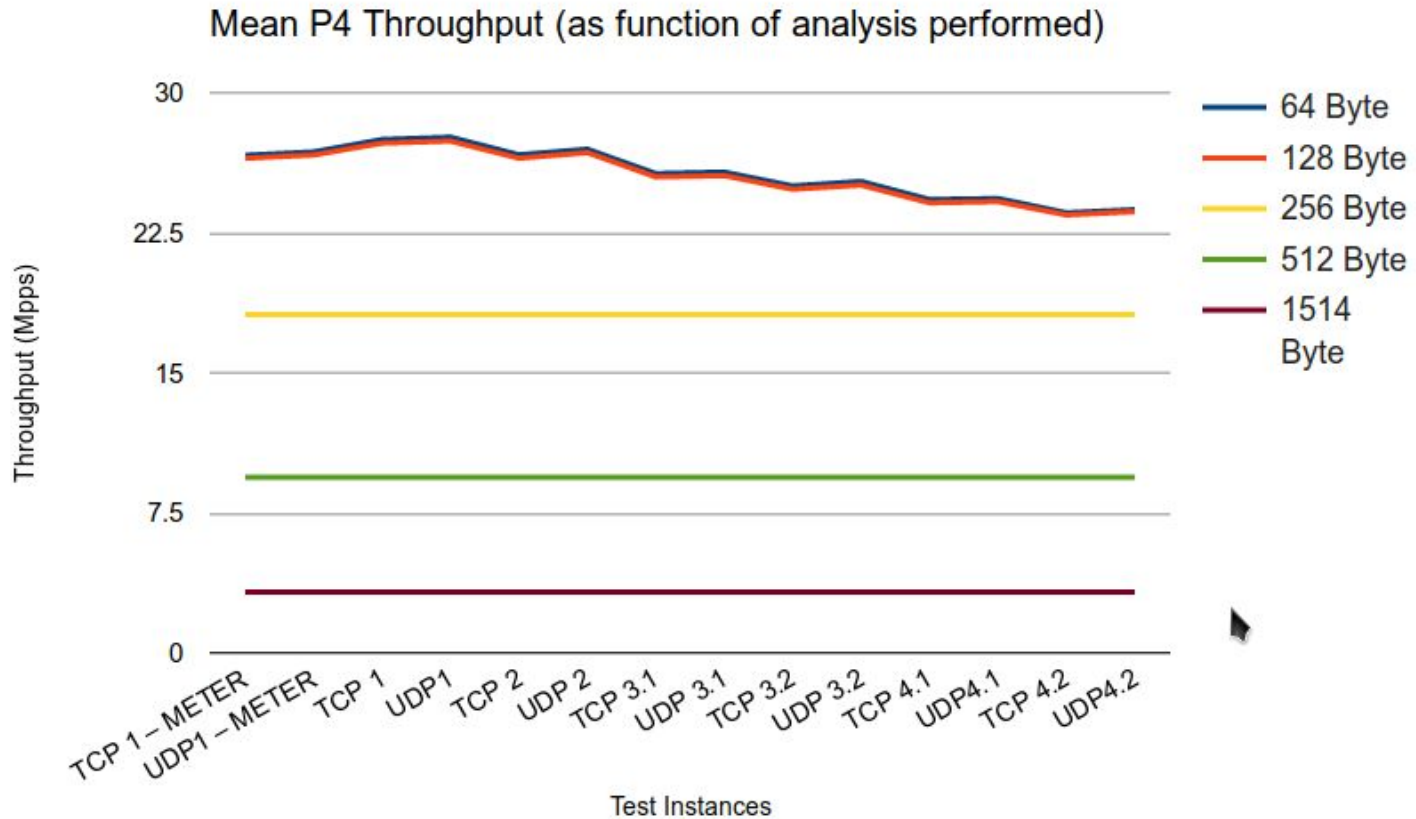
The screenshot displays the Netronome Programmer Studio interface. On the left, a C code editor shows the implementation of a P4 parser, including headers, parser functions for eth, ipv4, and ipv4 options, and a field list. In the center, a graphical data path (DP) view shows a flow from 'start' to 'eth_parse', then to 'ipv4_parse', and finally to 'ipv4_opt_parse' and 'valid(ipv4_opt)'. On the right, a console window shows the output of the build process, including the command 'P4 project setup complete.' and the path 'rnf-4xxx-b0 B0'.

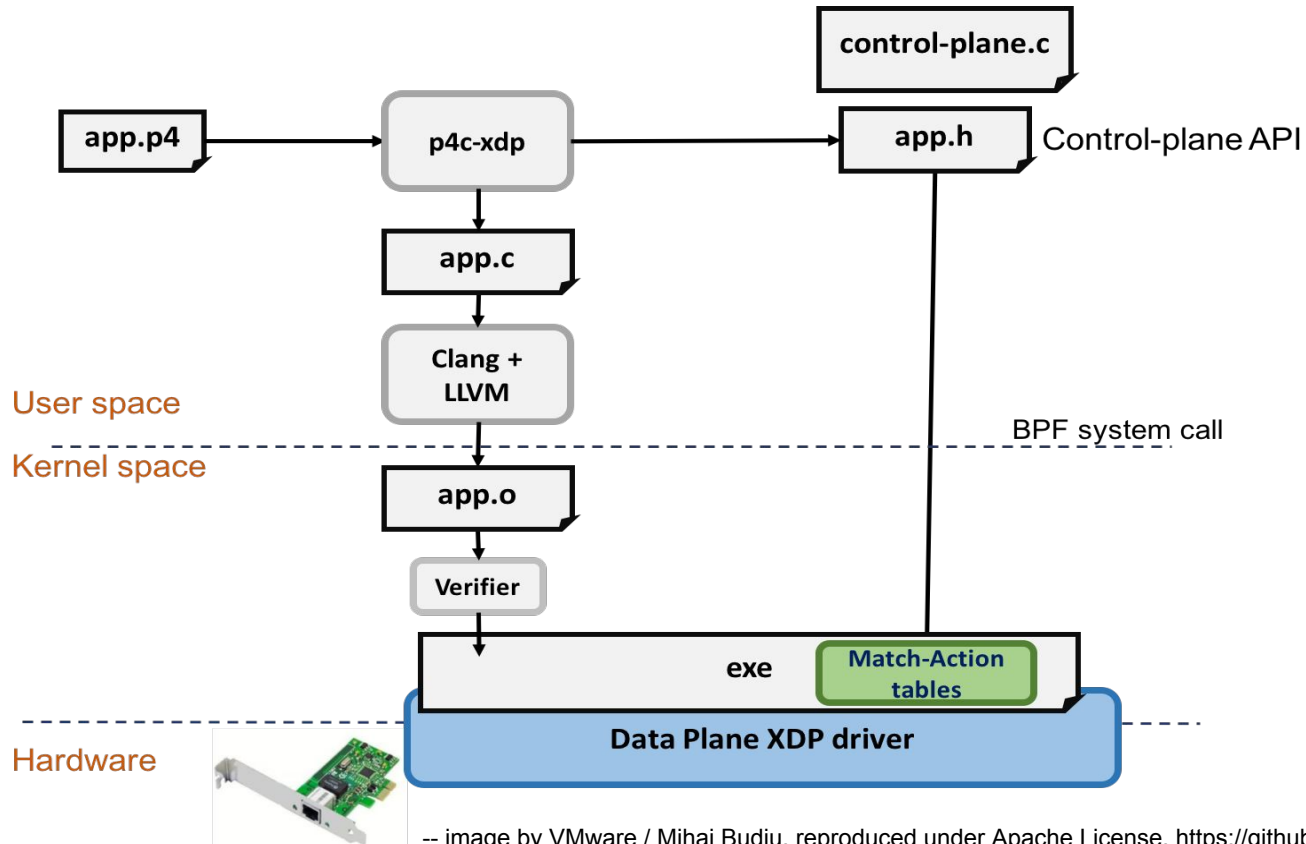
This screenshot shows the Netronome Programmer Studio interface with a focus on debugging. The top window displays a packet capture (pcap) of a P4 application, showing the 'parser_start' function and its subsequent calls to 'eth_parse', 'ipv4_parse', and 'ipv4_opt_parse'. Below the packet capture, a 'Registers' window shows the values of various registers, including 'RX', 'TX', and 'NFD'. On the right, a 'Memory Watches' window displays a table of memory addresses and their corresponding values.

CTM	EMEM	EMEM DC	IMEM	CLS	CTM	Crysto	ILA
0	4	8	12	16			
0x5a5a5a5a	0x5a5a5a5a	0x5a5a5a5a					









-- image by VMware / Mihai Budiu, reproduced under Apache License, <https://github.com/vmware/p4c-xdp>

- ▶ open-nfp.org

- ▶ Netronome white papers
 - www.netronome.com/media/redactor_files/WP_Programming_with_P4_and_C.pdf
 - www.netronome.com/media/redactor_files/WP_P4.pdf
 - www.netronome.com/media/redactor_files/WP_NFP_Programming_Model.pdf

- ▶ github.com/vmware/p4c-xdp

Questions?

A blurred person in a dark suit is walking past a modern glass building. The building features a prominent staircase with dark steps and a glass railing. The scene is brightly lit, suggesting an outdoor or well-lit indoor environment. The overall aesthetic is professional and modern.

NETRONOME

Thank You